IN THE CLAIMS

1. (Currently Amended) A flash memory device comprising:

a memory array with primary and redundant memory cells; and

redundant fuse circuitry used to replace the primary memory cells with the redundant memory cells, wherein the redundant fuse circuitry stores an error code indicating a type of defect in addition to a defect location.

2. (original) The flash memory device of claim 1 wherein the redundant fuse circuitry further stores the addresses of defective primary cells and compares the addresses with address requests to replace the primary memory cells with redundant memory cells.

3. (original) The flash memory device of claim 1 further comprising:

control circuitry to control memory operations to the memory array, wherein the control circuitry performs an erase operation algorithm that is specific to an error code in the redundant fuse circuitry.

4. (original) The flash memory device of claim 1 wherein the error code indicates a row to column short.

5. (original) The flash memory device of claim 1 wherein the error code indicates a row-to-row short.

6. (original) The flash memory device of claim 1 wherein the error code indicates an isolated defect.

7. (original) The flash memory device of claim 1 wherein the error code comprises two bits.

8. (Currently Amended) A flash memory device comprising:

at least one register to store an address of a defective element in a primary memory array, the register having at least one data bit to store an error code in addition to a defect location; and

a state machine to execute an algorithm based on the error code stored in the register.

9. (original) The flash memory device of claim 8 wherein the error code indicates a type of defect that is associated with the defective element in the primary memory array.

10. (original) The flash memory device of claim 8 wherein the error code comprises multiple bits.

11. (original) The flash memory device of claim 8 wherein the register includes a bank of either fuses, anti-fuses, or non-volatile cells.

12. (original) A flash memory device comprising:

a memory array;

redundant array elements;

a register for each redundant array element to store an address of a defective element in the memory array, each register further stores an error code;

a redundant circuit to redirect address requests from the defective element to an associated redundant array element; and

control circuitry to execute an algorithm based on the error code stored in the register.

13. (original) The flash memory device of claim 12 wherein the redundant element is a redundant row.

14. (original) The flash memory of claim 12 wherein the redundant element is a redundant column.

15. (original) The flash memory device of claim 12 wherein the algorithm controls an erase operation of the memory array.

16. (original) The flash memory of claim 12 wherein the redundant circuit redirects address requests from the at least one defective element to an associated redundant element when an address request matches an address in a register.

17. (original) A flash memory device comprising:

a memory array having memory cells arranged in columns and rows;

at least one redundant row coupled to the memory array to replace an associated defective row in the memory array; and

a register for each redundant row to store the address of the associated defective row, each register further stores an error code, wherein the error code indicates the type of error the redundant row is used to correct.

18. (original) The flash memory device of claim 17 further comprising:

a redundant circuit to redirect address requests from the defective row in the memory array to the redundant row.

19. (original) The flash memory device of claim 17 further comprising:

a state machine to control erase operations, the state machine having an algorithm that directs specific erase operations in response to an error code in a register.

20. (original) A flash memory device comprising:

a memory array having memory cells arranged in columns and rows;

at least one redundant column mapped to the memory array to replace an associated defective column in the memory array; and

a register for each redundant column to store the address of the associated defective column, each register having at least one extra bit to store an error code, wherein the error code indicates the type of error in the at least one defective column.

21. (original) The flash memory device of claim 20 further comprising:

a redundant circuit to redirect address requests from the defective column in the memory array to the associated redundant column.

22. (original) The flash memory device of claim 20 further comprising:

control circuitry to control erase operations, wherein the control circuitry directs specific erase operations in response to the type of error code stored in the register.

23. (original) The flash memory device of claim 20 wherein the error code comprises two bits.

24. (original) A flash memory device comprising:

a memory array having memory cells arranged in columns and rows;

at least one redundant row to replace an associated defective row in the memory array;

a register for each redundant row to store the address of an associated defective row, each register further having at least one bit to store an error code, wherein the error code indicates the type of defect in the associated defective row;

a redundant circuit to compare address requests to the addresses in the registers, wherein the redundant circuit directs address requests matching addresses in the registers to the associated redundant row instead of the defective row in the memory array; and

control circuitry to execute an erase operation algorithm based on the error code stored in each register.

25. (original) The flash memory system of claim 24 wherein the erase operation algorithm disables the redundant circuit during a pre-programming cycle and a soft programming cycle of an erase operation when the error code indicates a row to row short.

26. (original) The flash memory system of claim 25 wherein the control circuitry simultaneously programs the rows shorted together during the pre-programming cycle.

27. (original) The flash memory system of claim 25 wherein the control circuitry simultaneously applies a soft program pulse to the rows shorted together during the soft programming cycle if an over erased cell is detected in one of the rows.

28. (original) A flash memory device comprising:

a memory array having memory cells arranged in columns and rows;

at least one redundant row to replace an associated defective row in the memory array;

at least one redundant column to replace an associated defective column in the memory array; and

a register for each redundant row and each redundant column to store the addresses of associated defective rows and columns, each register having at least one bit to store an error code, wherein the error code indicates the type of defect the redundant row or column is used to correct.

29. (original) The flash memory device of claim 28 further comprising:

a first redundant circuit to redirect address requests from the defective column in the memory array to the associated redundant column; and

a second redundant circuit to redirect address requests from the defective row in the memory array to the associated redundant row.

30. (original) The flash memory device of claim 28 further comprising:

a state machine to control erase operations in response to the error code in a register.

31-56. (Canceled)